

## PATENT ABSTRACTS OF JAPAN

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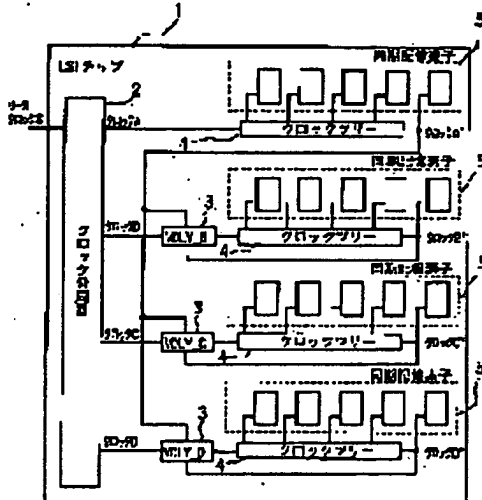
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## (54) SEMICONDUCTOR INTEGRATED CIRCUIT

## (57)Abstract:

PROBLEM TO BE SOLVED: To reduce a delay difference between clock signals at different frequencies without expansion by arranging a variable delay circuit, with which the phase difference of a reference clock signal and a clock signal supply source clock signal is matched, at the clock signal supply source of a clock signal system except for a reference clock signal system.

SOLUTION: A clock frequency divider 2 of an LSI chip 1 receives a source clock signal S and generates clock signals A-D at different frequencies. A clock tree 4 adjusts clock skew while receiving the correspondent clock signals B-D outputted from a variable delay circuit 3. The variable delay circuit 3 defines a clock signal A' to be the terminating clock signal of the clock signal system, to which the clock signal A at the lowest frequency is supplied, as the reference clock signal, compares the phases of the reference clock signal A' and terminating clock signals B'-D', matches the phase difference of the reference clock signal and the clock signals B-D and regulates the delay difference between signals into sufficiently small value.



## LEGAL STATUS

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## DETAILED DESCRIPTION

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### [Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the semiconductor integrated circuit equipped with the circuit group of the clock signal system of at least two or more different frequencies.

[0002]

[Description of the Prior Art] Conventionally, in the semiconductor integrated circuit which operates synchronizing with a clock signal, control of the clock skew in a single-clock signal is fully attained by application of a clock tree structure etc., and a circuit designer can perform a circuit design, without being conscious of clock skew. It is in the current semiconductor integrated circuit which is using the clock signal of a large number from which a frequency differs for the reasons of large-scale, a low power, etc. The clock signals A, B, C, and D which are generated from source clock signal S by the clock counting-down circuit 102 built in LSI chip 101 as shown in drawing 5 and with which frequencies differ, respectively It is adjusted so that clock skew may be lost with the clock trees 103A, 103B, 103C, and 103D which corresponded for every clock signal, respectively, and the synchronous storage element 104 of the circuit group of a clock signal system which corresponded, respectively is supplied.

[0003] However, since there was dispersion in delay between each clock tree 103A, 103B, and 103C and 103D, it was very difficult to decrease, so that each clock signal A, B, and C and the time delay difference between D can be disregarded with each clock tree 103A, 103B, 103C, and 103D. Furthermore, in modification of the layout of correction of the violation of timing generated according to this time delay difference of a circuit, when impossible, modification of circuitry, such as an algorithm, was needed and huge-ization of the development cycle of a circuit was caused. On the other hand, in order to avoid such fault, when the forecast of the time delay difference between different-species clock signals was designed greatly beforehand, insertion of a useless delay element and the component for making into a high speed that as which a circuit late originally is sufficient were added, and there was a possibility of causing the element number of the whole integrated circuit and increase of power consumption. Moreover, there was a possibility that circuit actuation might become unstable, by violation of timing by the time delay difference between the different-species clock signals produced by fluctuation of dispersion in a process, a temperature change, and supply voltage.

[0004] In order to solve such fault, as shown in drawing 6, each clock signal A and B on a board 105, LSI chip 106 which receives the clock signals A and B which were carried on the board 105 and corresponded, respectively -- PLL (phase locked loop circuit) 107 used in order to double the phase of each clock signal of the termination of A and B, as A and B are applied and it is shown in drawing 7. The clock signals A and B which are generated from source clock signal S by the clock counting-down circuit 109 built in LSI chip 108 and with which frequencies differ, respectively, Although \*\* which carries out phase doubling of the clock signal of the termination by which phase doubling was

carried out with the clock trees 110A and 110B which corresponded for every clock signal, respectively by PLL111A and B is also considered In such a case, in order PLL as shown in drawing 8 for every clock signal system is needed and to perform phase doubling of clock signals A and B, PLL is needed also for the interior of a counting-down circuit 109.

[0005]

[Problem(s) to be Solved by the Invention] If it was in the conventional semiconductor integrated circuit which is using many clock signals with which frequencies differ as explained above, reduction of the differential delay between each clock signal with which frequencies differ was very difficult. On the other hand, although the technique of reducing those differential delays using PLL can be considered, if it is in such technique, much PLL is needed and it is in causing the fault that circuitry is enlarged.

[0006] Then, the place which this invention is made in view of the above, and is made into that purpose reduces the differential delay between the clock signals with which frequencies differ, without causing enlargement of circuitry, and is to offer the semiconductor integrated circuit which improved stabilization of circuit actuation.

[0007]

[Means for Solving the Problem] In order to attain the above-mentioned purpose, invention according to claim 1 In the semiconductor integrated circuit equipped with the circuit group of the clock signal system of at least two or more different frequencies The clock signal which the clock signal input terminal of a clock signal receipt place which serves as termination of the clock signal of a clock signal system with the lowest frequency by said clock signal system is given is made into a reference clock signal. This reference clock signal, The clock signal of the clock signal supply origin in the clock signal system which corresponded, respectively, The termination clock signal fed back from said clock signal input terminal of the clock signal system which corresponded, respectively is received. The adjustable delay circuit with which the phase of a reference clock signal and a termination clock signal is compared with, and the phase contrast of a reference clock signal and the clock signal of the clock signal supply origin of the clock signal system which corresponds, respectively is doubled based on a comparison result It provides in the clock signal supply origin of the clock signal system except the clock signal system of a reference clock signal, the differential delay between the clock signals with which frequencies differ, without causing enlargement of circuitry compared with the case where PLL is used is reduced, and it is characterized by raising stabilization of circuit actuation.

[0008] Invention according to claim 2 said adjustable delay circuit The phase comparator which compares the phase of both signals in a semiconductor integrated circuit according to claim 1 in response to said reference clock signal and said termination clock signal, The loop filter which generates the control voltage signal according to the phase contrast of a reference clock signal and a termination clock signal based on the comparison result of said phase comparator, The control voltage signal generated with said loop filter and the clock signal of said clock signal supply origin are received. It has the armature-voltage control delay circuit which carries out delay control of the clock signal of clock signal supply origin based on a control voltage signal, and is characterized by attaining the miniaturization of circuitry compared with the case where PLL is used.

[0009] Invention according to claim 3 is characterized by providing the counting-down

circuit which generates the clock signal of each of said clock signal system in response to a source clock signal in a semiconductor integrated circuit according to claim 1 or 2.

[0010]

[Embodiment of the Invention] Hereafter, the gestalt of implementation of this invention is explained using a drawing.

[0011] Drawing 1 is drawing showing the configuration of the semiconductor integrated circuit concerning 1 operation gestalt of invention according to claim 1, 2, or 3.

[0012] In drawing 1 LSI chip 1 of the semiconductor integrated circuit of this operation gestalt The clock counting-down circuit 2 which generates four clock signals A, B, C, and D with which frequencies differ in response to source clock signal S, respectively from the exterior, The adjustable delay circuit 3 which is prepared respectively corresponding to the clock signals B, C, and D generated with the clock counting-down circuit 2, and adjusts the phase of clock signals B, C, and D (VDL\_B, VDL\_C, VDL\_D), The clock tree 4 which adjusts clock skew in response to the clock signals B, C, and D which are outputted, and which corresponded, respectively from clock signal A or the adjustable delay circuit 3, It has the synchronous storage element 5 which constitutes the circuit county of each clock signal system from a clock input terminal in response to the termination clock signal (clock signal A', B', C', D') of each clock tree 4, and is constituted.

[0013] the termination clock signal of a clock signal system with which, as for the adjustable delay circuit 3, lowest clock signal A of the inside of clock signals A, B, C, and D and a frequency is supplied, and clock signal [ becoming ] A -- ' -- a reference clock signal -- carrying out -- this reference clock signal -- The clock signals B, C, and D which were generated with the clock counting-down circuit 2 and which correspond, respectively, Clock signal B' used as the termination clock signal of a clock signal system which corresponded, respectively, C', and D' are received. The phase of a reference clock signal and a termination clock signal is compared, the phase contrast of a reference clock signal and clock signals B, C, and D is doubled based on a comparison result, and the differential delay between each signal is adjusted to a sufficiently small value. Such an adjustable delay circuit 3 is formed between the output of the clock counting-down circuit 2 which becomes the clock signal supply origin of each clock signal system except the clock signal system which set up the reference clock signal, and the input of the clock tree 4 which corresponds, respectively.

[0014] Since a reference clock signal turns into a signal of the clock input terminal of all the synchronous storage elements 5 driven with the termination clock signal of the clock tree 4 which receives clock signal A, two or more synchronous storage elements 5 and same numbers will exist, but since the clock skew in the clock signal system of clock signal A is adjusted to the value small enough by the corresponding clock tree 4, its one clock signal of arbitration may be enough for being used as a reference clock signal. Or the termination clock signal of the clock tree 4 of the clock signal system of clock signal A is merged, and it may be made to consider as one reference clock signal. The clock counting-down circuit 2 is deleted and you may make it, give clock signals A, B, C, and D from the exterior to direct LSI chip 1 on the other hand, as shown in drawing 2 .

[0015] In such a configuration, the clock signals A, B, C, and D which dividing of the source clock signal S was carried out by the clock counting-down circuit 2, and were generated and with which frequencies differ, respectively are adjusted to a sufficiently

small value by the adjustable delay circuit 3 established in each clock signal system except the clock signal system of clock signal A from which the differential delay between each signal serves as a reference clock signal, and are supplied to the clock input terminal of the synchronous storage element 5 of the circuit county of a clock signal system which corresponded, respectively. The time delay difference between different-species clock signals can be correctly assumed in the phase of designing the semiconductor integrated circuit which uses by this two or more clock signals with which frequencies differ, and the circuit where the timing of a clock signal was optimized can be designed. Moreover, since dispersion in a process and the time delay difference between the different-species clock signals produced by fluctuation of a temperature change or supply voltage are reduced, a manufacture margin can be made small, the yield improves and it becomes possible to also guarantee service conditions, such as temperature and supply voltage, in the large range.

[0016] Moreover, since actuation of the adjustable delay circuit 3 of this operation gestalt is limited as the Prior art explained, Compared with PLL, as for the adjustable delay circuit 3, the miniaturization of a configuration is attained even at one half extent. And (the -one number of clock signals) is sufficient as the number of the adjustable delay circuit 3 for which the adjustable delay circuit 3 becomes unnecessary at the clock signal system of a reference clock signal, and is needed, and circuitry can be sharply miniaturized compared with the case where PLL is simply used by all clock signal systems by these. Furthermore, as shown in drawing 2 , when the clock counting-down circuit 2 does not need to be mounted in LSI chip 1, it is not necessary to make correctly in agreement the phase between two or more different-species clock signals inputted into LSI chip 1, and a design becomes easy.

[0017] Drawing 3 is drawing showing the concrete circuitry of the adjustable delay circuit 3 shown in drawing 1 or drawing 2 .

[0018] In drawing 3 , the adjustable delay circuit 3 is realized by transposing VCO of PLL shown in drawing 9 to an electrical-potential-difference adjustable delay circuit (VD). the phase comparator (PD) which compares both phase and outputs a rise signal (UP) or a down signal (DOWN) according to a comparison result in response to a reference clock signal and the termination clock signal fed back from the clock tree 4 -- six -- In response to the rise signal or down signal outputted from a phase comparator 6, charge or discharge is performed based on the signal except the high frequency component of these signals. the loop filter (LP) which generates the control signal electrical potential difference (Vcot) according to the phase contrast of both the signals compared with the phase comparator 6 -- seven -- The clock signal with which the clock signals B, C, and D given from the clock counting-down circuit 2 or the outside corresponded, and the control voltage signal generated with the loop filter 7 are received. It has the electrical-potential-difference adjustable delay circuit (VD) 8 which doubles the phase contrast of a clock signal and a reference clock signal according to a control voltage signal, and adjusts the time delay difference between both signals to a value small enough, and is constituted.

[0019] In such a configuration, the phase of a reference clock signal and a termination clock signal is compared by the phase comparator 6. When the phase of a termination clock signal is progressing rather than the reference clock signal, a down signal is outputted to a loop filter 7 from a phase comparator 6. When the phase of a termination

clock signal is behind the reference clock signal, a rise signal is outputted to a loop filter 7 from a phase comparator 6. The control voltage signal which discharge will be performed by loop-formation FURUTA 7 and will delay the phase of a clock signal if a down signal is outputted is given to the electrical-potential-difference adjustable control circuit 8. If a rise signal is outputted, the control voltage signal which charge is performed by loop-formation FURUTA 7 and advances the phase of a clock signal will be given to the electrical-potential-difference adjustable control circuit 8, the phase of a clock signal is delayed or advanced by these control voltage signals, and the phase contrast between both signals is adjusted.

[0020] As shown in drawing 4, it is constituted by the MOS transistor, and cascade connection of the inverter 9 of CMOS and the inverter 11 of CMOS by which the control voltage signal was connected to the high order power source VDD through the transistor 10 of the P channel given to the gate terminal is carried out, and the electrical-potential-difference adjustable delay circuit 8 is constituted, as shown in this drawing (A) or this drawing (B). thus, since it can be easy and can constitute small, compared with the conventional PLL, the electrical-potential-difference adjustable delay circuit 8 can be boiled markedly, and can miniaturize the adjustable delay circuit 3.

[0021]

[Effect of the Invention] Without causing enlargement of circuitry compared with the case where PLL is used according to this invention, as explained above, the differential delay between the clock signals with which frequencies differ can be reduced, and stabilization of circuit actuation can be raised.

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## TECHNICAL FIELD

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[Field of the Invention] This invention relates to the semiconductor integrated circuit equipped with the circuit group of the clock signal system of at least two or more different frequencies.

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## PRIOR ART

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[Description of the Prior Art] Conventionally, in the semiconductor integrated circuit which operates synchronizing with a clock signal, control of the clock skew in a single-clock signal is fully attained by application of a clock tree structure etc., and a circuit designer can perform a circuit design, without being conscious of clock skew. It is in the current semiconductor integrated circuit which is using the clock signal of a large number from which a frequency differs for the reasons of large-scale, a low power, etc. The clock signals A, B, C, and D which are generated from source clock signal S by the clock counting-down circuit 102 built in LSI chip 101 as shown in drawing 5 and with which frequencies differ, respectively It is adjusted so that clock skew may be lost with the clock trees 103A, 103B, 103C, and 103D which corresponded for every clock signal,

respectively, and the synchronous storage element 104 of the circuit group of a clock signal system which corresponded, respectively is supplied.

[0003] However, since there was dispersion in delay between each clock tree 103A, 103B, and 103C and 103D, it was very difficult to decrease, so that each clock signal A, B, and C and the time delay difference between D can be disregarded with each clock tree 103A, 103B, 103C, and 103D. Furthermore, in modification of the layout of correction of the violation of timing generated according to this time delay difference of a circuit, when impossible, modification of circuitry, such as an algorithm, was needed and huge-ization of the development cycle of a circuit was caused. On the other hand, in order to avoid such fault, when the forecast of the time delay difference between different-species clock signals was designed greatly beforehand, insertion of a useless delay element and the component for making into a high speed that as which a circuit late originally is sufficient were added, and there was a possibility of causing the element number of the whole integrated circuit and increase of power consumption. Moreover, there was a possibility that circuit actuation might become unstable, by violation of timing by the time delay difference between the different-species clock signals produced by fluctuation of dispersion in a process, a temperature change, and supply voltage.

[0004] In order to solve such fault, as shown in drawing 6, each clock signal A and B on a board 105, LSI chip 106 which receives the clock signals A and B which were carried on the board 105 and corresponded, respectively -- PLL (phase locked loop circuit) 107 used in order to double the phase of each clock signal of the termination of A and B, as A and B are applied and it is shown in drawing 7. The clock signals A and B which are generated from source clock signal S by the clock counting-down circuit 109 built in LSI chip 108 and with which frequencies differ, respectively, Although \*\* which carries out phase doubling of the clock signal of the termination by which phase doubling was carried out with the clock trees 110A and 110B which corresponded for every clock signal, respectively by PLL 111A and B is also considered. In such a case, in order PLL as shown in drawing 8 for every clock signal system is needed and to perform phase doubling of clock signals A and B, PLL is needed also for the interior of a counting-down circuit 109.

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## EFFECT OF THE INVENTION

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[Effect of the Invention] Without causing enlargement of circuitry compared with the case where PLL is used according to this invention, as explained above, the differential delay between the clock signals with which frequencies differ can be reduced, and stabilization of circuit actuation can be raised.

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## TECHNICAL PROBLEM

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[Problem(s) to be Solved by the Invention] If it was in the conventional semiconductor integrated circuit which is using many clock signals with which frequencies differ as explained above, reduction of the differential delay between each clock signal with which

frequencies differ was very difficult. On the other hand, although the technique of reducing those differential delays using PLL can be considered, if it is in such technique, much PLL is needed and it is in causing the fault that circuitry is enlarged.

[0006] Then, the place which this invention is made in view of the above, and is made into that purpose reduces the differential delay between the clock signals with which frequencies differ, without causing enlargement of circuitry, and is to offer the semiconductor integrated circuit which improved stabilization of circuit actuation.

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## MEANS

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[Means for Solving the Problem] In order to attain the above-mentioned purpose, invention according to claim 1 In the semiconductor integrated circuit equipped with the circuit group of the clock signal system of at least two or more different frequencies The clock signal which the clock signal input terminal of a clock signal receipt place which serves as termination of the clock signal of a clock signal system with the lowest frequency by said clock signal system is given is made into a reference clock signal. This reference clock signal, The clock signal of the clock signal supply origin in the clock signal system which corresponded, respectively, The termination clock signal fed back from said clock signal input terminal of the clock signal system which corresponded, respectively is received. The adjustable delay circuit with which the phase of a reference clock signal and a termination clock signal is compared with, and the phase contrast of a reference clock signal and the clock signal of the clock signal supply origin of the clock signal system which corresponds, respectively is doubled based on a comparison result It provides in the clock signal supply origin of the clock signal system except the clock signal system of a reference clock signal, the differential delay between the clock signals with which frequencies differ, without causing enlargement of circuitry compared with the case where PLL is used is reduced, and it is characterized by raising stabilization of circuit actuation.

[0008] Invention according to claim 2 said adjustable delay circuit The phase comparator which compares the phase of both signals in a semiconductor integrated circuit according to claim 1 in response to said reference clock signal and said termination clock signal, The loop filter which generates the control voltage signal according to the phase contrast of a reference clock signal and a termination clock signal based on the comparison result of said phase comparator, The control voltage signal generated with said loop filter and the clock signal of said clock signal supply origin are received. It has the armature-voltage control delay circuit which carries out delay control of the clock signal of clock signal supply origin based on a control voltage signal, and is characterized by attaining the miniaturization of circuitry compared with the case where PLL is used.

[0009] Invention according to claim 3 is characterized by providing the counting-down circuit which generates the clock signal of each of said clock signal system in response to a source clock signal in a semiconductor integrated circuit according to claim 1 or 2.

[0010]

[Embodiment of the Invention] Hereafter, the gestalt of implementation of this invention is explained using a drawing.

[0011] Drawing 1 is drawing showing the configuration of the semiconductor integrated circuit concerning 1 operation gestalt of invention according to claim 1, 2, or 3.

[0012] In drawing 1 LSI chip 1 of the semiconductor integrated circuit of this operation gestalt The clock counting-down circuit 2 which generates four clock signals A, B, C, and D with which frequencies differ in response to source clock signal S, respectively from the exterior, The adjustable delay circuit 3 which is prepared respectively corresponding to the clock signals B, C, and D generated with the clock counting-down circuit 2, and adjusts the phase of clock signals B, C, and D (VDL\_B, VDL\_C, VDL\_D), The clock tree 4 which adjusts clock skew in response to the clock signals B, C, and D which are outputted, and which corresponded, respectively from clock signal A or the adjustable delay circuit 3, It has the synchronous storage element 5 which constitutes the circuit county of each clock signal system from a clock input terminal in response to the termination clock signal (clock signal A', B', C', D') of each clock tree 4, and is constituted.

[0013] the termination clock signal of a clock signal system with which, as for the adjustable delay circuit 3, lowest clock signal A of the inside of clock signals A, B, C, and D and a frequency is supplied, and clock signal [ becoming ] A -- ' -- a reference clock signal -- carrying out -- this reference clock signal -- The clock signals B, C, and D which were generated with the clock counting-down circuit 2 and which correspond, respectively, Clock signal B' used as the termination clock signal of a clock signal system which corresponded, respectively, C', and D' are received. The phase of a reference clock signal and a termination clock signal is compared, the phase contrast of a reference clock signal and clock signals B, C, and D is doubled based on a comparison result, and the differential delay between each signal is adjusted to a sufficiently small value. Such an adjustable delay circuit 3 is formed between the output of the clock counting-down circuit 2 which becomes the clock signal supply origin of each clock signal system except the clock signal system which set up the reference clock signal, and the input of the clock tree 4 which corresponds, respectively.

[0014] Since a reference clock signal turns into a signal of the clock input terminal of all the synchronous storage elements 5 driven with the termination clock signal of the clock tree 4 which receives clock signal A, two or more synchronous storage elements 5 and same numbers will exist, but since the clock skew in the clock signal system of clock signal A is adjusted to the value small enough by the corresponding clock tree 4, its one clock signal of arbitration may be enough for being used as a reference clock signal. Or the termination clock signal of the clock tree 4 of the clock signal system of clock signal A is merged, and it may be made to consider as one reference clock signal. The clock counting-down circuit 2 is deleted and you may make it, give clock signals A, B, C, and D from the exterior to direct LSI chip 1 on the other hand, as shown in drawing 2 .

[0015] In such a configuration, the clock signals A, B, C, and D which dividing of the source clock signal S was carried out by the clock counting-down circuit 2, and were generated and with which frequencies differ, respectively are adjusted to a sufficiently small value by the adjustable delay circuit 3 established in each clock signal system except the clock signal system of clock signal A from which the differential delay between each signal serves as a reference clock signal, and are supplied to the clock input terminal of the synchronous storage element 5 of the circuit county of a clock signal system which corresponded, respectively. The time delay difference between different-

species clock signals can be correctly assumed in the phase of designing the semiconductor integrated circuit which uses by this two or more clock signals with which frequencies differ, and the circuit where the timing of a clock signal was optimized can be designed. Moreover, since dispersion in a process and the time delay difference between the different-species clock signals produced by fluctuation of a temperature change or supply voltage are reduced, a manufacture margin can be made small, the yield improves and it becomes possible to also guarantee service conditions, such as temperature and supply voltage, in the large range.

[0016] Moreover, since actuation of the adjustable delay circuit 3 of this operation gestalt is limited as the Prior art explained, Compared with PLL, as for the adjustable delay circuit 3, the miniaturization of a configuration is attained even at one half extent. And (the -one number of clock signals) is sufficient as the number of the adjustable delay circuit 3 for which the adjustable delay circuit 3 becomes unnecessary at the clock signal system of a reference clock signal, and is needed, and circuitry can be sharply miniaturized compared with the case where PLL is simply used by all clock signal systems by these. Furthermore, as shown in drawing 2 , when the clock counting-down circuit 2 does not need to be mounted in LSI chip 1, it is not necessary to make correctly in agreement the phase between two or more different-species clock signals inputted into LSI chip 1, and a design becomes easy.

[0017] Drawing 3 is drawing showing the concrete circuitry of the adjustable delay circuit 3 shown in drawing 1 or drawing 2 .

[0018] In drawing 3 , the adjustable delay circuit 3 is realized by transposing VCO of PLL shown in drawing 9 to an electrical-potential-difference adjustable delay circuit (VD). the phase comparator (PD) which compares both phase and outputs a rise signal (UP) or a down signal (DOWN) according to a comparison result in response to a reference clock signal and the termination clock signal fed back from the clock tree 4 -- six -- In response to the rise signal or down signal outputted from a phase comparator 6, charge or discharge is performed based on the signal except the high frequency component of these signals. the loop filter (LP) which generates the control signal electrical potential difference (Vcot) according to the phase contrast of both the signals compared with the phase comparator 6 -- seven -- The clock signal with which the clock signals B, C, and D given from the clock counting-down circuit 2 or the outside corresponded, and the control voltage signal generated with the loop filter 7 are received. It has the electrical-potential-difference adjustable delay circuit (VD) 8 which doubles the phase contrast of a clock signal and a reference clock signal according to a control voltage signal, and adjusts the time delay difference between both signals to a value small enough, and is constituted.

[0019] In such a configuration, the phase of a reference clock signal and a termination clock signal is compared by the phase comparator 6. When the phase of a termination clock signal is progressing rather than the reference clock signal, a down signal is outputted to a loop filter 7 from a phase comparator 6. When the phase of a termination clock signal is behind the reference clock signal, a rise signal is outputted to a loop filter 7 from a phase comparator 6. The control voltage signal which discharge will be performed by loop-formation FURUTA 7 and will delay the phase of a clock signal if a down signal is outputted is given to the electrical-potential-difference adjustable control circuit 8. If a rise signal is outputted, the control voltage signal which charge is

performed by loop-formation FURUTA 7 and advances the phase of a clock signal will be given to the electrical-potential-difference adjustable control circuit 8, the phase of a clock signal is delayed or advanced by these control voltage signals, and the phase contrast between both signals is adjusted.

[0020] As shown in drawing 4 , it is constituted by the MOS transistor, and cascade connection of the inverter 9 of CMOS and the inverter 11 of CMOS by which the control voltage signal was connected to the high order power source VDD through the transistor 10 of the P channel given to the gate terminal is carried out, and the electrical-potential-difference adjustable delay circuit 8 is constituted, as shown in this drawing (A) or this drawing (B). thus, since it can be easy and can constitute small, compared with the conventional PLL, the electrical-potential-difference adjustable delay circuit 8 can be boiled markedly, and can miniaturize the adjustable delay circuit 3.

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## DESCRIPTION OF DRAWINGS

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### [Brief Description of the Drawings]

[Drawing 1] It is drawing showing the configuration of the semiconductor integrated circuit concerning 1 operation gestalt of invention according to claim 1, 2, or 3.

[Drawing 2] It is drawing showing the configuration of the semiconductor integrated circuit concerning 1 operation gestalt of invention according to claim 1 or 2.

[Drawing 3] It is drawing showing the configuration of an adjustable delay circuit.

[Drawing 4] It is drawing showing one configuration of an electrical-potential-difference adjustable delay circuit.

[Drawing 5] It is drawing showing the configuration of the conventional semiconductor integrated circuit which is using two or more clock signals with which frequencies differ.

[Drawing 6] It is drawing showing the configuration of the conventional semiconductor integrated circuit with which PLL is used for the circuit shown in drawing 5 .

[Drawing 7] It is drawing showing the configuration of the semiconductor integrated circuit which two or more PLL was used by the circuit shown in drawing 5 , and was formed into 1 chip.

[Drawing 8] It is drawing showing the configuration of PLL.

### [Description of Notations]

1 LSI Chip

2 Clock Counting-down Circuit

3 Adjustable Delay Circuit

4 Clock Tree

5 Synchronous Storage Element

6 Phase Comparator

7 Loop Filter

8 Armature-voltage Control Delay Circuit

9, 11, 14, 15 Inverter

10, 12, 13 Transistor

**\* NOTICES \***

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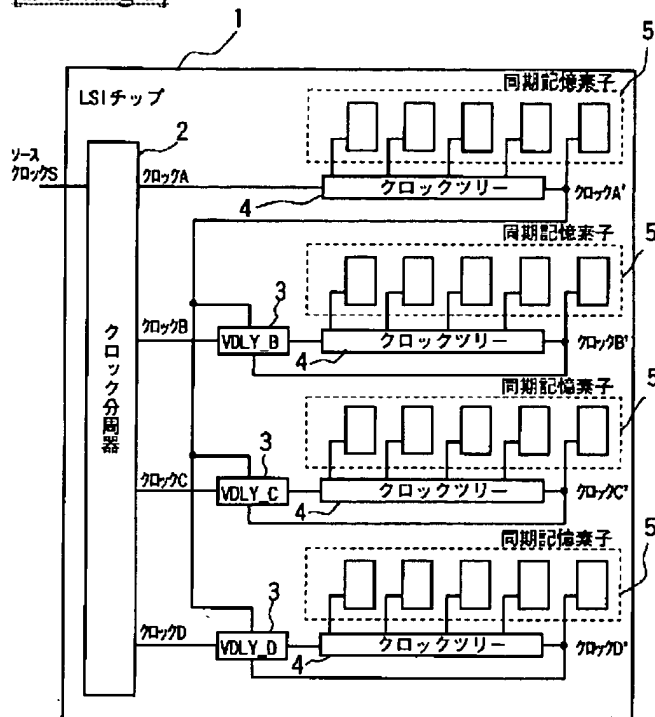
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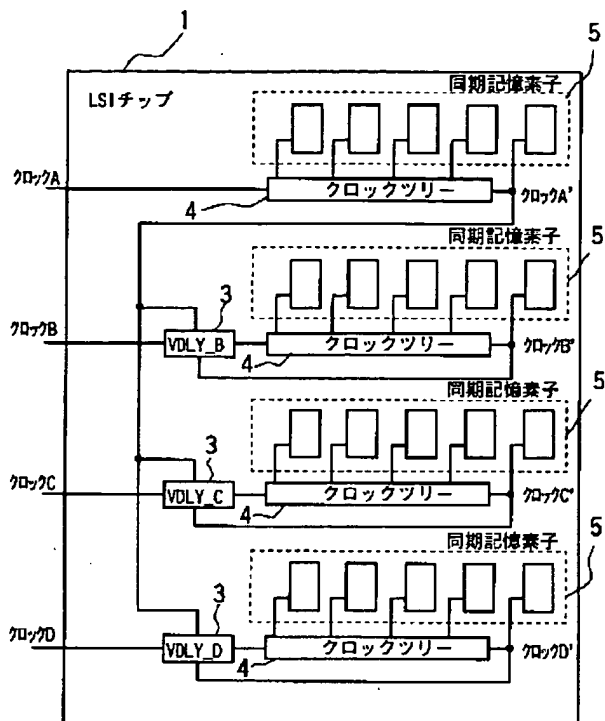
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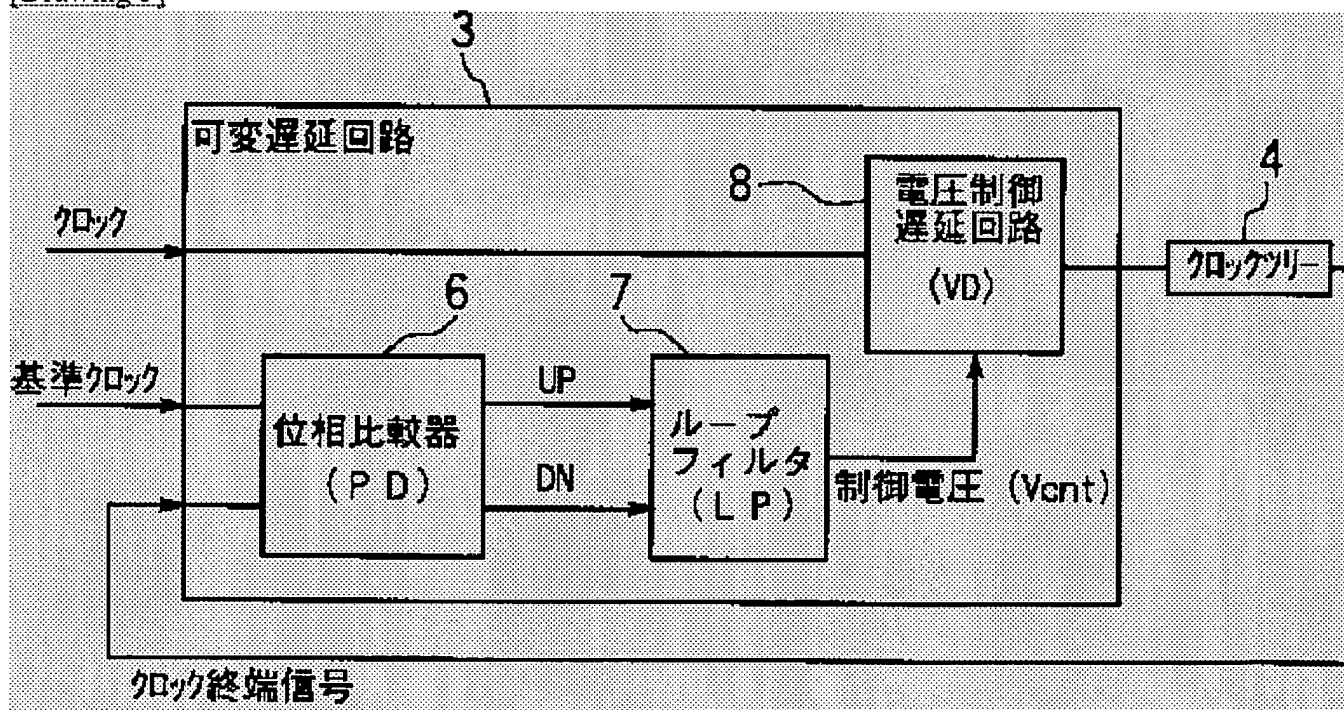
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[Drawing 2]

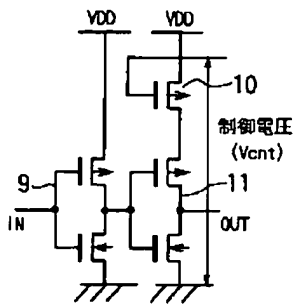


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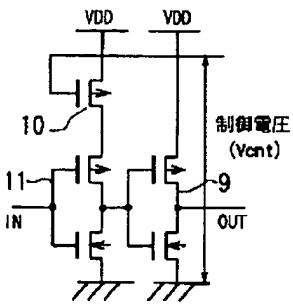


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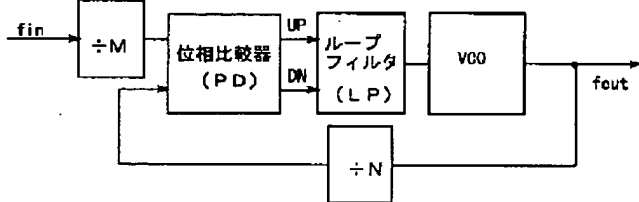
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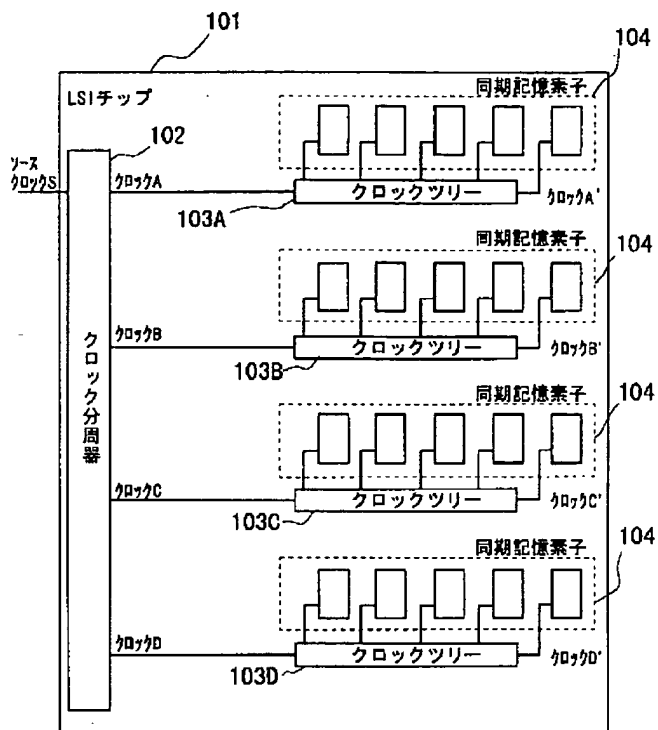
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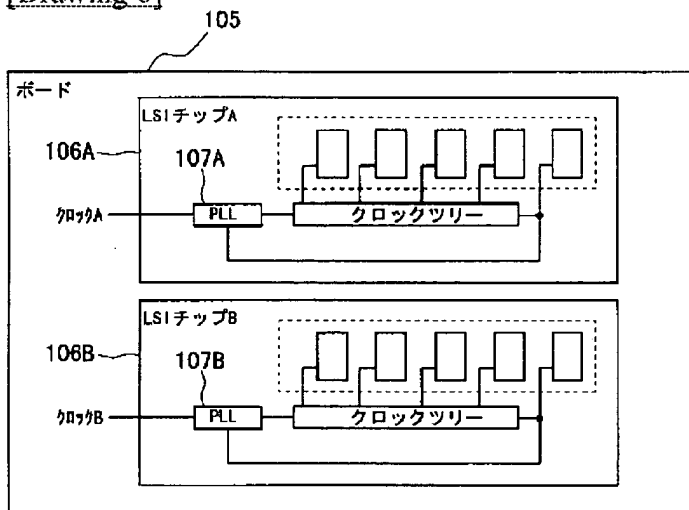
[Drawing 8]



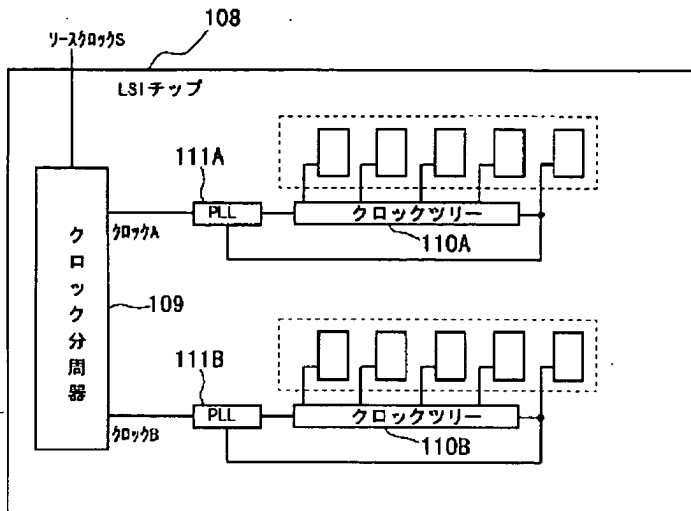
[Drawing 5]



[Drawing 6]



[Drawing 7]



## CLAIMS

### [Claim(s)]

[Claim 1] In the semiconductor integrated circuit equipped with the circuit group of the clock signal system of at least two or more different frequencies The clock signal which the clock signal input terminal of a clock signal receipt place which serves as termination of the clock signal of a clock signal system with the lowest frequency by said clock signal system is given is made into a reference clock signal. This reference clock signal, The clock signal of the clock signal supply origin in the clock signal system which corresponded, respectively, The termination clock signal fed back from said clock signal input terminal of the clock signal system which corresponded, respectively is received. The adjustable delay circuit with which the phase of a reference clock signal and a termination clock signal is compared with, and the phase contrast of a reference clock signal and the clock signal of the clock signal supply origin of the clock signal system which corresponds, respectively is doubled based on a comparison result The semiconductor integrated circuit characterized by providing in the clock signal supply origin of the clock signal system except the clock signal system of a reference clock signal.

[Claim 2] The phase comparator with which said adjustable delay circuit compares the phase of both signals in response to said reference clock signal and said termination clock signal, The loop filter which generates the control voltage signal according to the phase contrast of a reference clock signal and a termination clock signal based on the comparison result of said phase comparator, The semiconductor integrated circuit according to claim 1 characterized by having the armature-voltage control delay circuit which carries out delay control of the clock signal of clock signal supply origin based on a control voltage signal in response to the control voltage signal generated with said loop filter, and the clock signal of said clock signal supply origin.

[Claim 3] The semiconductor integrated circuit according to claim 1 or 2 characterized by

providing the counting-down circuit which generates the clock signal of each of said clock signal system in response to a source clock signal.

1.

wherein said first and second signal paths have substantially the same wiring conductor length.

2. A semiconductor integrated circuit according to Claim 1, wherein said first circuit block has an output latch circuit for latching the data signal to be transmitted, said second circuit block has an input

latch circuit for latching the data signal to be received, and said output latch circuit and said input latch circuit are configured to perform the latch operation in response to the clock signals before and after, respectively, being transmitted from said first circuit block to said second circuit block.

3. A semiconductor integrated circuit according to Claim 2, wherein said first circuit block is configured to send the next data signal and the clock signal to said first and second signal paths before arrival of the transmitted data signal clock signal at said second circuit block.

4. A semiconductor integrated circuit according to Claim 1, wherein said second circuit block includes a plurality of circuits operated in synchronism with the internal clock generated based on the clock signal received from said second signal path, and said clock distribution line pattern of said second circuit block is configured to distribute said internal clock to said plurality of circuits through the substantially same length of path.

5. A semiconductor integrated circuit according to Claim 4, wherein said circuit blocks are configured in such a manner that when said data signal is not sent out to said second circuit block from said first circuit block, said clock signal is not sent out from said first circuit block to said second circuit block.

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6. A semiconductor integrated circuit according to Claim 1, wherein a third signal path for feeding back the clock signal received by said second circuit block to said first circuit block is inserted between said first and second circuit blocks, and said first circuit block includes a phase adjusting circuit for adjusting the phase of the clock signal sent out from said first circuit block in such a manner that the clock signal in said first circuit block is in phase with the clock signal fed back.

7. A semiconductor integrated circuit according to Claim 6, wherein said phase adjusting circuit includes a phase detecting circuit for generating a phase difference signal representing the phase difference obtained by comparing the phase of the clock signal in said first circuit block with the phase of said clock signal fed back, and variable delay circuits with the delay time thereof variable based on the phase difference signal from said phase detecting circuit.

8. A semiconductor integrated circuit according to Claim 1, wherein said second circuit block includes a plurality of circuits operated in synchronism with a clock signal different from said clock signal received, and the clock distribution line pattern of said second circuit block is configured to distribute said different clock signal to said plurality of the circuits through paths having substantially the same length.

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9. A semiconductor integrated circuit according to Claim 8, wherein said second circuit block includes means for taking the serial data signal received from said first signal path, based on the received clock signal and storing said serial data signal for at least two periods of said received clock signal, and means for reading the data signal stored in said storage means by a clock signal different from said received clock signal.

10. A semiconductor integrated circuit according to Claim 9,

wherein said second circuit block includes a phase shifting circuit for generating a clock signal out of phase by one half period of the data transmission cycle based on the received clock, and a phase adjusting circuit for generating a clock signal giving a timing of taking data to said holding means based on the clock signal generated by said phase shifting circuit, and

wherein said phase adjusting circuit operates to adjust the phase of the clock signal supplied to said holding means in such a manner that the clock signal generated by said phase-shifting circuit is in phase with the phase of the clock signal supplied to said holding means.

11. A semiconductor integrated circuit according to Claim 10, wherein said holding means is configured

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to take said received data signal substantially at the center between the changing points of said received data signal.

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